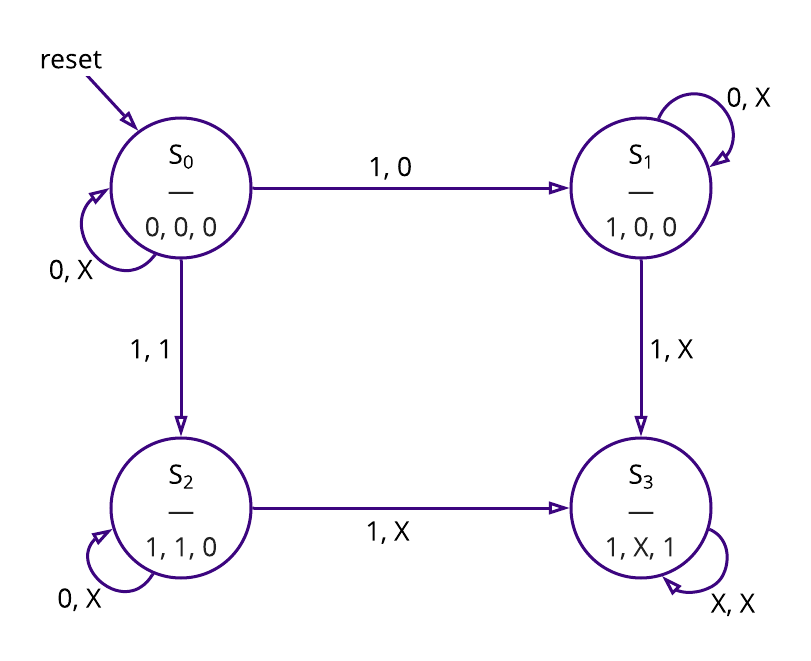
Project by – Vijay dwivedi (2020csb1140) and Tanish Goyal (2020csb1133)

**Idea 1 - Tic tac toe**

**Objective –** Implementing the Tic tac toe using the Verilog code and simulating the code

**Functionality** - Tic-tac-toe is a classic game with a grid layout of nine cells. Two players, represented by X and O, fill one square with their symbol until one player wins or a draw is reached. A win is achieved when the player fills three adjacent cells in a particular combination with his/her symbol.

**Implementation** – There are 4 states – S0 , S1, S2, S3



2 Inputs – mark and player.

3 outputs – marked owner and error.

**States**

The first state, S0, indicates that the square is empty and has not been used yet.

state S1, which will output that the square has been marked and indicate which player marked it.

S2 where the outputs indicate that the square is marked by this player.

Finally, the control unit will go to S3 if either player attempted to mark an occupied square. This state will output error as well as indicate the marked status of the square.

**Idea 2 – Image processing**

**Objective –** Implementing the Image processing using Verilog and simulating the code.

**Functionality** - processing operations are implemented in Verilog such as inversion, brightness control and threshold operations.

**Implementation** –

The image processing operation is selected by a "parameter.v" file and then, the processed image data are written to a bitmap image output.bmp for verification purposes.

As Verilog can not read images directly . The Image is required to convert from bitmap format to the hexadecimal format. We can convert it using Matlab.

We will separate the RGB values. Then we will use known algorithm for filters like greyscale, sepia, and blur etc.

**Idea 3 – Digital delay Timer**

**Objective** Implementing the Digital delay timer using Verilog and simulating the code.

**Functionality -** Basically, the delay timer has 4 operating modes: one-shot (OS), Delayed Operate (DO), Delayed Release(DR), Dual Delay (DD).

**Implementation –** it encorporates time delay ranges. These ranges produce real-time delays when the input time-base frequency is within 10 kHz to 1 kHz. It has an ac oscillator port for time-base generation and complementary delay outputs with an option to "flash" one output as a delay-in progress indicator. Delays are initiated by a trigger and can be aborted by a reset.

